REMARKS

A. Status of the Claims

Claims 1-31 are pending in the application. Claims 4 and 20-24 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2 and 4-5 of US Patent No. 6,635,556 (hereinafter the '556 patent) in view of Wang et al., US Patent No. 6,511,923. Claims 7, 8, 10-12, and 15-19 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-14 of the '556 patent in view of Choi, US Patent No. 5,950,109.

Claims 1-3, 5, 25-28, and 30-31 were rejected under 35 USC 102(c) as being anticipated by Wang et al. Claim 15 was rejected under 35 USC 102(c) as being anticipated by Wang et al..

Claims 6, 16-18, 20-23, and 29 were rejected under 35 USC 103(a) as being unpatentable over Wang et al. in view of Hill, US Patent Application No. 6,384,466. Claims 7-13 were rejected under 35 USC 103(a) as being unpatentable over Wang et al. in view of Choi. Claim 14 was rejected under 35 USC 103(a) as being unpatentable over Wang et al. in view of Choi and further in view of Hill.

B. Obviousness-Type Double Patenting Claim Rejections: Claims 4 and 20-24

Claims 4 and 20-24 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2 and 4 5 of the '556 patent (the parent of the present application) in view of Wang et al.

Claim 4 recites a method of making a semiconductor device comprising: forming a first in-situ doped silicon layer over a substrate material in a pressure vessel while

introducing a precursor gas; without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the doped silicon layer; and removing the undoped silicon capping layer; further comprising, after the step of removing the undoped silicon capping layer, depositing a second in-situ doped silicon layer, wherein the first doped layer is formed with an n-type dopant or a p-type dopant, and the second doped layer is formed with a p-type dopant or an n-type dopant, the type of the second layer opposite the type of the first doped layer. (This summary includes the limitations of claim 4 and those of claims 1 and 3, from which it depends.)

Claim 1 of US Patent No. the '556 patent recites a method of making a silicon-based electronic device comprising the steps of: forming a first doped silicon layer in a pressure vessel over a surface of a product wafer substrate material while introducing a precursor gas, the first doped layer comprising n-type or p-type silicon; without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on the first doped silicon layer, the undoped silicon capping layer having a thickness sufficient to reduce autodoping to approximately a back-ground level; and forming a next doped silicon layer on the undoped silicon capping layer, the next doped layer comprising p-type or n-type silicon, the type opposite the type of the first doped layer.

A difference between claim 4 of the present invention and claim 1 of the '556 patent is the inclusion of a step to remove the undoped silicon capping layer. The Examiner points to Wang et al. (col. 6, lines 40-48) for this teaching, saying:

> Wang discloses a method for forming a stable dielectric films (sic) comprises the step of removing the undoped silicon capping layer 18 by CMP.

Applicants respectfully point out, however, that layer 18 of Fig. 2 of Wang et al. (referred to in the passage cited by the Examiner) is not in fact an undoped silicon capping layer. This layer is a dielectric material such as "silicon oxide, silicon nitride, silicon oxynitride, and the like," (col. 5, lines 48-50), not silicon. These materials are insulators, unlike silicon, which is a semiconductor.

The Examiner continues:

> One skilled in the art at the time the invention was made would have found it obvious to modify claims 1-2, 4-5 of US 6,635,556 by adding the step of removing the undoped silicon capping layer as per Wang to produce instant claim inventions as per claims 4, 20-24 because Wang discloses that a planarization procedure such as CMP is common after dielectric deposition prior to subsequent processing ...

The Examiner is correct that Wang et al. teach that CMP is commonly performed after dielectric deposition. But the crucial element of the claim is that a portion of an undoped *silicon* layer is removed. Wang et al. teach that the CMP step removes overfill of dielectric layer 20 and a portion of dielectric layer 18, but not another material such as silicon. In fact, Wang et al. point out, at col. 6, line 48-50:

> More typically, planarization is performed at a level slightly above the upper surfaces of the islands 14 ...

In other words, a CMP step like the one taught by Wang et al. typically removes only dielectric fill like oxides, nitrides, or oxynitrides, and stops before reaching any other material. Thus the combination of Wang et al. with claim 1 of the '556 patent would not result in the invention of claims 4 and 20-24.

Applicants respectfully request withdrawal of the double-patenting obviousness-type rejection of claim 4.

Claim 20 of the present invention recites a method of making a silicon-based electronic device comprising the steps of: forming a first doped silicon layer in a pressure

vessel over a surface of a product wafer substrate material while introducing a precursor gas; and without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the first doped silicon layer, wherein the layers form a portion of a three dimensional memory array.

The Examiner rejected claims 20-24 using the same rationale as that used to reject claim 4 of the present application. Applicants suspect, however, that these claims may have been included in error, as none of claim 20 nor its dependent claims 21-24 includes a step of removing a silicon capping layer. Further, neither Wang et al. nor any of claims 1-2 or 4-5 refers to a three dimensional memory array, as recited in claim 21. Applicants respectfully request clarification.

C. Obviousness-Type Double Patenting Claim Rejections: Claims 7, 8, 10-12, and 15-19

Claims 7, 8, 10-12 and 15-19 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-14 of the '556 patent in view of Choi.

Claim 7 recites a method of conditioning a pressure vessel to prevent autodoping, the method comprising the steps of: forming a first doped silicon layer in the pressure vessel over a surface of a first wafer while introducing a precursor gas; without removing the first wafer from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the first doped silicon layer and on exposed surfaces in the pressure vessel; and introducing a second wafer into the pressure vessel after formation of the undoped capping layer and forming a

second silicon layer over a surface of the second wafer, wherein the thickness of the undoped capping layer is sufficient to reduce autodoping in the second silicon layer to approximately a background level.

Claim 11 of the '556 patent recites a method of making a silicon-based electronic device comprising the steps of: forming a first doped layer over a substrate by in-situ doping silicon with n-type or p-type dopant atoms; forming an undoped silicon capping layer on the first doped layer, the silicon capping layer having a thickness sufficient to reduce autodoping to approximately a background level; and forming a second doped layer on the capping layer by in-situ doping silicon with p-type or n-type dopant atoms, the dopant type the opposite of the first doped layer, wherein the steps of forming the first doped layer and forming the silicon capping layer take place without removing the substrate from a chamber.

A difference between claim 7 of the present application and claim11 of the '556 patent is that the second doped layer is deposited on a second wafer, not on the first wafer. The Examiner says:

> Choi discloses a method for depositing films on semiconductor wafer comprises [sic] the step of introducing a second wafer into the pressure vessel and forming a second silicon layer over the surface of the second wafer ...

First, Applicants note that Choi describes deposition of films on semiconductor wafers using a chemical vapor deposition method, but at no point identifies those film as silicon films; indeed, the word "silicon" does not appear in Choi. Choi does mention, as an example, deposition of silica glass (col. 5, line 17), but silica glass is not silicon; it is SiO_2.

The Examiner continues:

> One skilled in the art at the time the invention was made would have found it obvious to modify claims 11-14 of US 6,635,556 by adding the step of introducing a second wafer into the pressure vessel and forming a second silicon layer over the surface of the second wafer as per Choi ... because Choi discloses that his invention eliminates the need to use dummy wafers and allows the repeated, efficient and continuous loading of sets of active wafers into a deposition apparatus ...

Briefly, the invention of Choi is a method to avoid the use of dummy wafers. Choi describes that when a film is being deposited on a wafer in a chamber having a number of dispersion heads, the wafer is moved from head to head so that an equal fraction of the final thickness of the film is deposited while the wafer is on each dispersion head. For example, in a chamber having five dispersion heads, D/H A, D/H B, D/H C, D/H D, and D/H E, one-fifth of the film deposition on a product wafer takes place on D/H A, then the product wafer is moved to D/H B, where the next one-fifth of the film deposition takes place, and so on, until the film deposition on the product wafer is completed on the fifth dispersion head, D/H E. The process is mechanized, so each wafer starts at D/H A and moves through D/H E, then is removed. Presumably none of the dispersion heads can be empty during operation, so when operation begins, the first product wafer is on D/H A, and the other four dispersion heads must also be occupied. While the first product wafer progresses from D/H A to D/H E, the other wafers must advance ahead of it, and be removed ahead of it. Because these wafers will not actually occupy all five heads, they will not receive the full intended thickness. Thus they cannot be used as product wafers, and are dummy wafers. Similarly, the wafers that follow the last product wafer receiving a full deposition thickness receive only a partial thickness, and are also dummy wafers.

The invention of Choi is apparently to reintroduce the wafers which received only a partial deposition in place of the dummy wafers in such order that they receive the full intended film thickness and can be used as product wafers, thus avoiding the use of dummy wafers and resulting waste. In the passage cited by the Examiner (col. 5, lines 25-30), Choi is describing an embodiment in which a first group of wafers receives a first film thickness, the leading wafer is removed (though retained for reintroduction later), the other wafers advanced, and a new wafer introduced; then a second firm thickness is deposited.

There are central differences in the steps described by Choi which make it first, sufficiently different from both claim 11 of the '556 patent and claim 7 of the present application that the suggested combination cannot produce the elements of claim 7; and, second, irrelevant to claim 11 of the '556 patent, such that one skilled in the art would have no reason to look to Choi to make the suggested modification.

First, it is central to the invention of Choi that the first and second layers of a deposition, and indeed all layers, be of the same material. Choi makes it clear that what is deposited in each step is a percentage of a final film thickness which must eventually be uniform; thus each layer is the *same* material (col. 2, lines 35-54, e.g., and col. 4, lines 38-50.) In both claim 7 of the present application and claim 11 of the '556 patent, though, the first and second layers, and the undoped capping layer, are all different materials (the undoped capping layer is undoped silicon, while the first and second layers are silicon of opposite doping types.) Thus claim 11 of the '556 application cannot logically be combined with the methods of Choi.

In addition, Applicants point out that claim 7 of the present application recites a method of conditioning a pressure vessel to prevent autodoping. Thus one skilled in the art would have no reason to look to Choi, which does not mention use of different doping types in subsequent depositions, and neither mentions the problem of autodoping nor suggests a solution, for guidance. There is no motivation to turn to Choi to modify claim 11 of the '556 patent. As claim 11 of the '556 patent and Choi cannot be combined, and there is no motivation to combine them, Applicants respectfully request withdrawal of the obviousness-type double patenting rejection of claims 7-8, 10-12, and 15-19.

D. 35 USC 102(e) Claim Rejections: Claims 1-3, 5, 25-28, and 30-31

Claims 1-3, 5, 25-28, and 30-31 were rejected under 35 USC 102(e) as being anticipated by Wang et al. Claim 1 recites a method of making a semiconductor device comprising: forming a first in-situ doped silicon layer over a substrate material in a pressure vessel while introducing a precursor gas; without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the doped silicon layer; and removing the undoped silicon capping layer.

To summarize, the claim requires a first doped silicon layer and an undoped silicon capping layer. The Examine identifies layer 16 of Wang et al. as "a first in-situ dielectric layer 16/doped silicon layer ..." and layer 18 of Wang et al. as "an undoped silicon capping layer."

As described in section B of these remarks, layer 18 of Wang et al. is not a silicon layer; it is rather a dielectric layer such as silicon dioxide, silicon nitride, or silicon oxynitride. Similarly, layer 16 is identified by Wang et al. as, for example, fluorine-

doped delicate glass or carbon-doped porous silicon dioxide (col. 5, lines 10-13.) In any case layer 16 is a "dielectric material having a dielectric constant that is lower than that of a conventional silicon oxide layer," (col. 5, lines 7-8.) As doped silicon is conductive, layer 16 cannot be doped silicon as required by the claim.

Thus the teachings of Wang et al. do not anticipate claim 1 or its dependent claims 3 and 5.

Claim 25 includes the limitation that the undoped silicon capping layer may be removed or consumed. As noted, Wang et al. do not teach deposition of a first doped, silicon layer or deposition of an undoped silicon capping layer, and also do not teach an undoped silicon capping layer being removed or consumed, and thus cannot anticipate claim 25 or its dependent claims 26-28 and 30-31.

Applicants respectfully request reconsideration.

E. 35 USC 102(e) Claim Rejections: Claim 15

Claim 15 was rejected under 35 USC 102(e) as being anticipated by Wang et al. Claim 15 recites a method of making a silicon-based electronic device comprising the steps of: forming a first doped silicon layer in a pressure vessel over a surface of a product wafer substrate material while introducing a precursor gas; without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the first doped silicon layer; and forming a second doped silicon layer on and in contact with the undoped silicon capping layer, wherein the layers form a portion of a memory device.

As described in sections B and of these Remarks, Wang et al. describe deposition of a dielectric layer such as silicon dioxide, silicon nitride, or silicon oxynitride, but do

not describe deposition of a first doped silicon layer, an undoped silicon capping layer, or a second doped silicon layer, as in claim 15; thus the teachings of Wang et al. do not anticipate claim 15. Applicants respectfully request reconsideration.

F. 35 USC 103(a) Claim Rejections: Claims 6, 16-18, 20-23, and 29

Claims 6, 16-18, 20-23, and 29 were rejected under 35 USC 103(a) as being unpatentable over Wang et al. in view of Hill.

Claim 6 recites a method of making a semiconductor device comprising: forming a first in-situ doped silicon layer over a substrate material in a pressure vessel while introducing a precursor gas; without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the doped silicon layer; and removing the undoped silicon capping layer, further comprising, after the step of removing the undoped silicon capping layer, depositing a second in-situ doped silicon layer, wherein the doped layers form a portion of a memory device, wherein the memory device forms a portion of a three dimensional memory array.

As in earlier rejections, the Examiner finds doped and undoped silicon layers in Wang et al. As explained above, Wang et al. in fact teach deposition of dielectric layers, not of doped or undoped silicon layers. Thus, even without considering the teachings of Hill, the combined references cannot teach or suggest each and every element of the claims. Applicants request reconsideration.

G. 35 USC 103(a) Claim Rejections: Claims 7-13

Claims 7-13 were rejected under 35 USC 103(a) as being unpatentable over Wang et al. in view of Choi.

As described above, Wang et al. do not teach deposition of silicon layers, and thus the combined references do not teach or suggest each and every element of the claims. Applicants respectfully request reconsideration.

H. 35 USC 103(a) Claim Rejections: Claim 14

Claim 14 was rejected under 35 USC 103(a) as being unpatentable over Wang et al. in view of Choi and further in view of Hill.

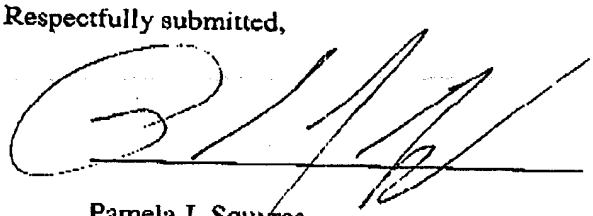
As described above, Wang et al. do not teach deposition of silicon layers, and thus the combined references do not teach or suggest each and every element of the claims. Applicants respectfully request reconsideration.

CONCLUSION

In light of this response, Applicants believe this application to be in condition for allowance. If there are any questions concerning this response, the Examiner is invited to contact the undersigned agent at (408) 869-2921.

Dated: July 14, 2005

Respectfully submitted,



Pamela J. Squyres
Agent for Applicants
Reg. No. 52,246

Matrix Semiconductor
3230 Scott Blvd
Santa Clara, CA 95054
Tel. 408-869-2921